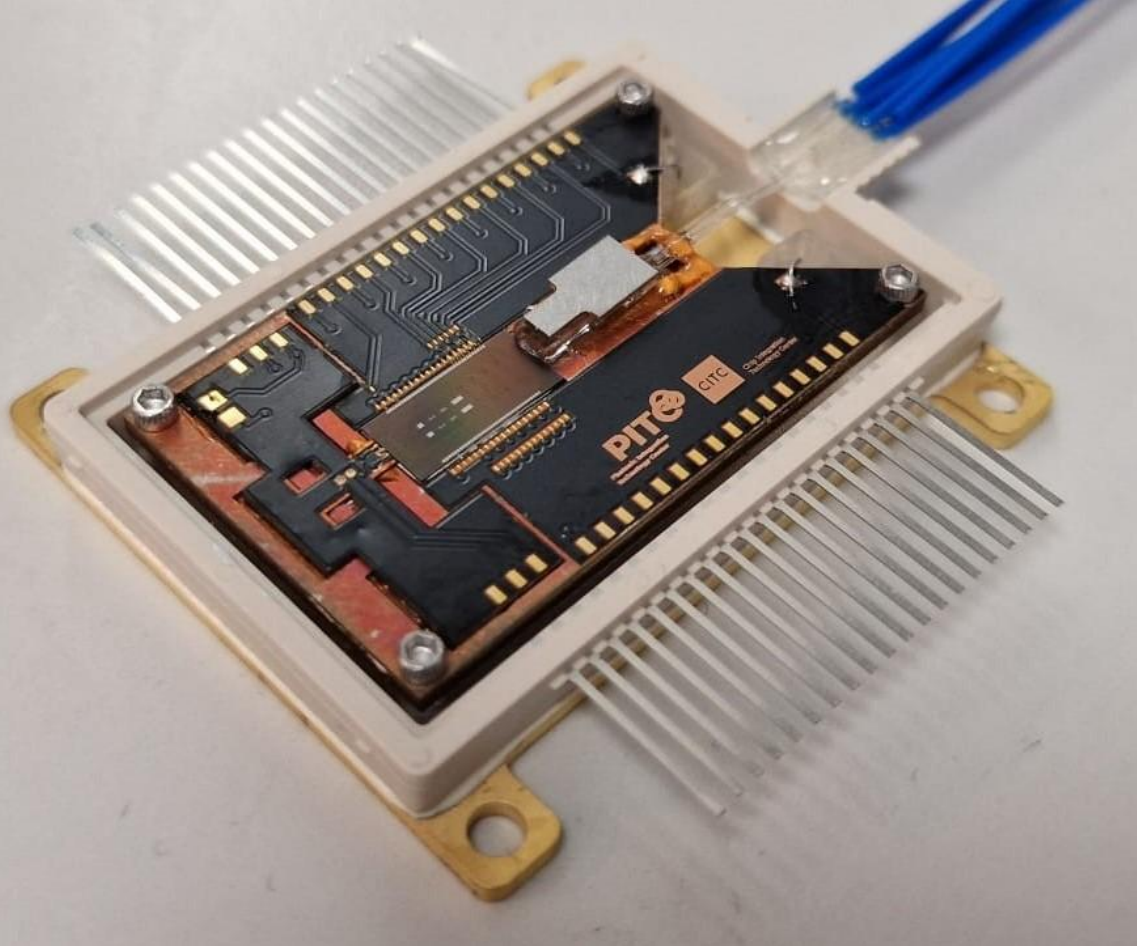




PITC.NL

PITC Introduction

Accelerating Integrated Photonics by bridging the gap between research and application

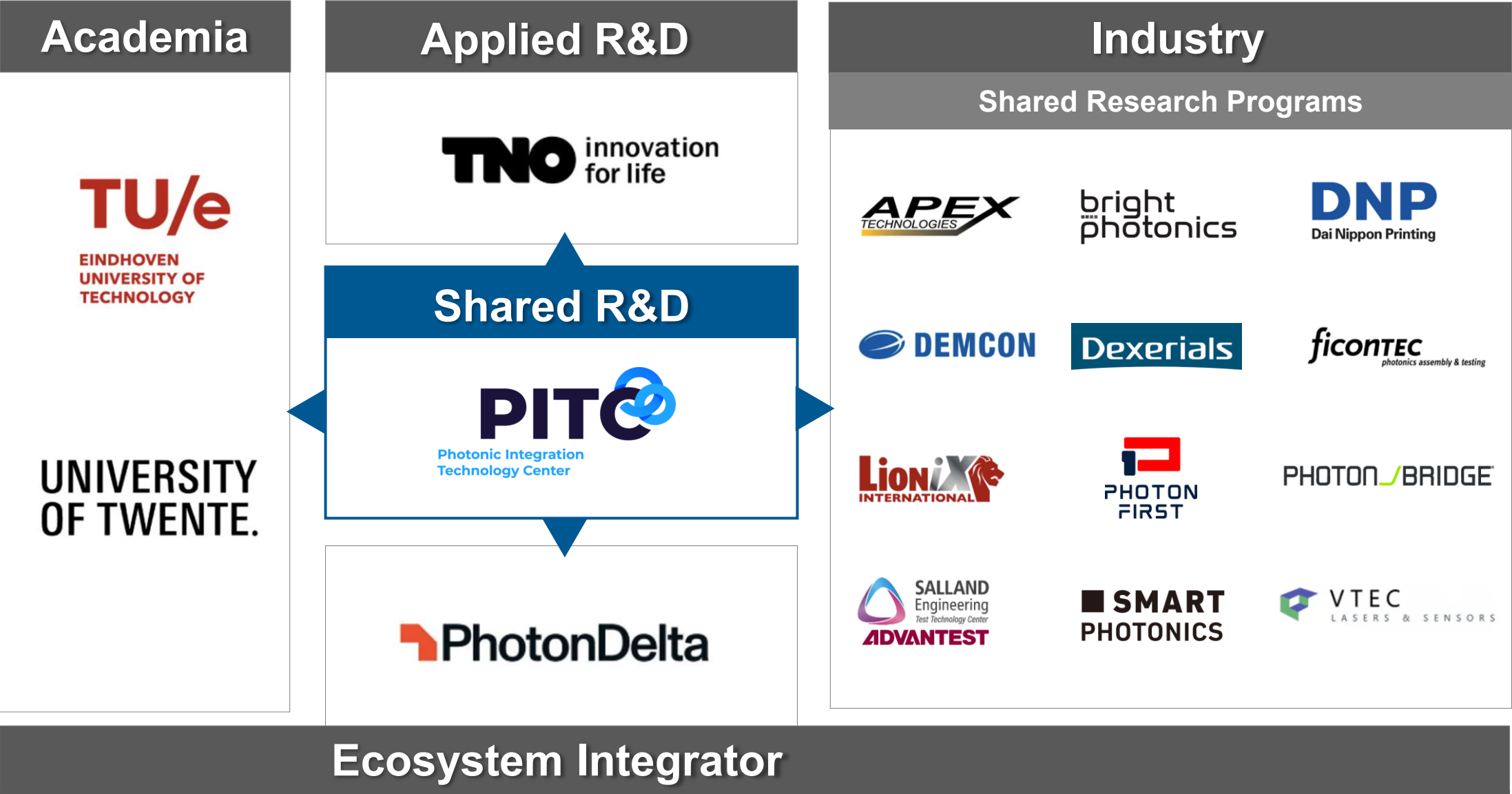
Takeshi Kamijo, R&D Scientist, TNO-PITC
Brabant Innovation Day, June 9, 2026 in Tokyo

We are part of the European innovation ecosystem for **photonics**.

We develop technologies that connect the world of **chips** with the world of **light**.

Our work enables **faster communication** and new opportunities for **healthcare, and industry**.

PITC Parties and Participants



Value Proposition of PITC Shared R&D Programs



Whom do we want to serve?

Companies across or entering the photonics and semiconductor value chain

The Need we want to address

Access to key enabling technologies of tomorrow with a reasonable investment of budget and engineering capacity.

Participants' Benefits

Shared investment, shared learning, shared results.

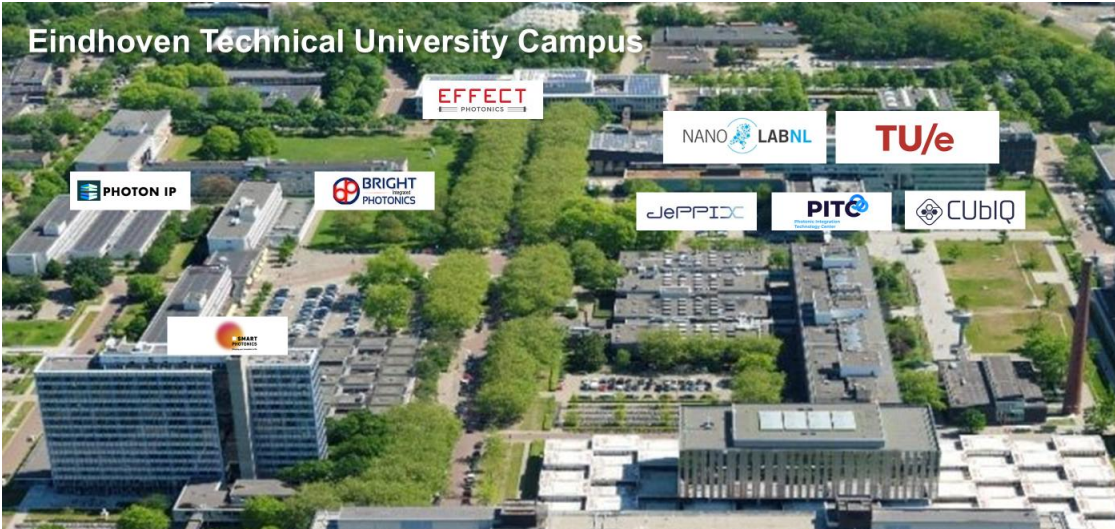
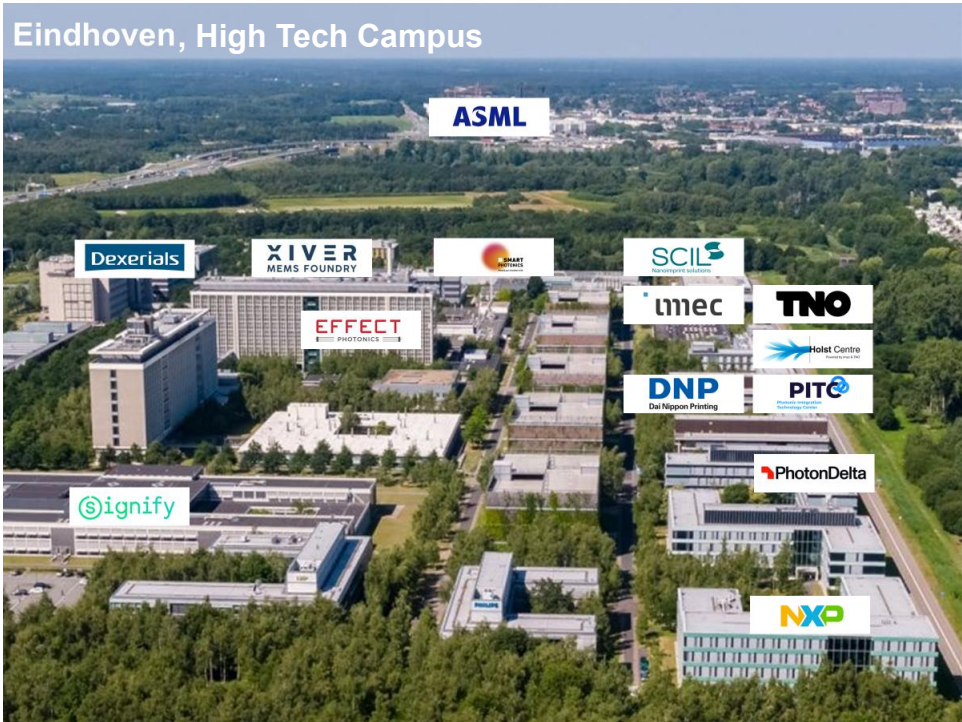
Earlier industrial readiness with lower risk and lower cost

Core PITC Assets

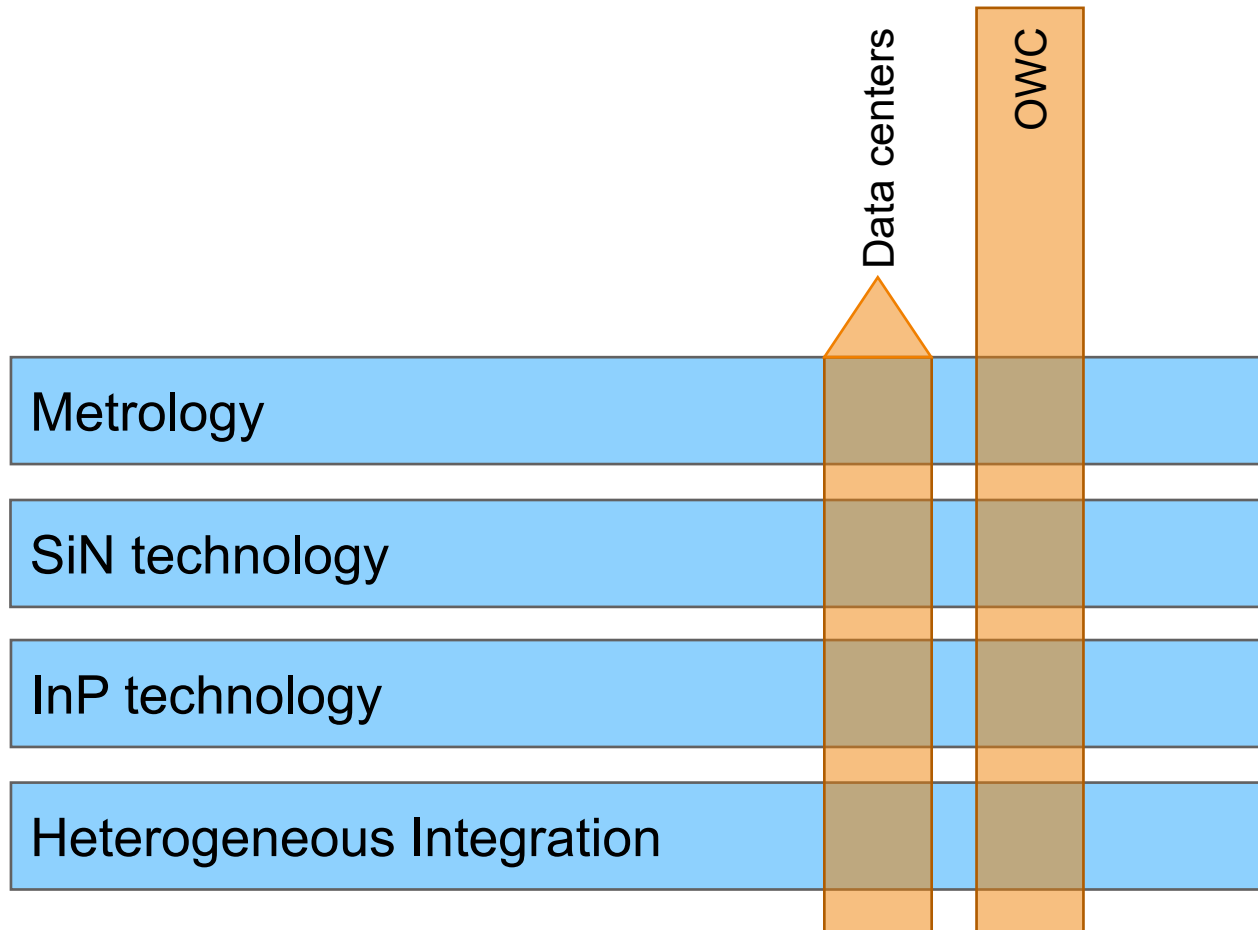
A proven ecosystem-driven industrialization model

Built on 20+ years of experience with Shared R&D Model with 100+ participants

Core Asset: Dutch Integrated Photonics Ecosystem Proximity



PITC Shared Research Programs



- We work along a technology roadmap with industrially relevant proof points.
- Yearly updated work plan together with program partners.
- Technology development is executed by teams of the PITC founders and industrial partners.
- Over 40 FTEs and growing, supported by expertise-on-demand from PITC founders

PITC SiN Program

Low loss SiN waveguides

- For quantum and microwave photonics applications
- Target: <0.01 dB/cm with excellent reproducibility

Integration of ultra-low power modulators on SiN

- Stress based modulators for quasi-DC application
- Target: $<1\mu\text{W}$ per modulator
- Direct e-o modulation through heterogeneous integration
- V_{π} (@1 mm) <5 Volt and switching speed $\gg 10$ GHz

Coupling strategies for low-loss SiN PICs

- Alignment-tolerant low loss Fiber to SiN chip coupling. Target: insertion loss < 0.5 dB



PITC InP Program

Creating custom InP building blocks

- Advancing fields like LiFi, LiDAR, and communication applications
- High performance of optical amplifiers, lasers and modulators

Developing manufacturing technologies

- Towards next-generation manufacturing nodes
- Significantly larger wafer sizes
- InP coupons fabrication

Equipment: AIXTRON MOCVD (12x4”), DUV ASML (193nm)



Heterogeneous Integration Program

PANEL LEVEL PACKAGING FOR CO-PACKAGED OPTICS (CPO)

HIGHLY SCALABLE, COST-EFFICIENT ADVANCED GLASS INTERPOSER TECHNOLOGY

PITC Heterogeneous Integration Program

- Co-packaged optics based on scalable panel level integration holds **great promise** to realize lower energy consumption, high-speed and cost-effective data transmission in datacom industry, **directing our targets and ambitions.**

Fast and high-precision assembly by LIFT

Targets are:

- Placement accuracy: +/- 200 nm
- >10,000 components/min

High-precision assembly
technology

Optical RDL based on polymer waveguide

Targets are:

- Low loss fiber-to-chip coupling with <1 dB.
- Relaxed alignment tolerance with micron-level accuracy.

Flat-panel technology

TGVs and Electrical RDL for electrical interconnects

Targets are:

- Denser and 3D EIC integration.
- Chip-last, Chip-first RDL
- New TGVs metallization method.

Flat-panel technology
Printing technology

PITC Metrology Program

Wafer-scale optical and electrical testing

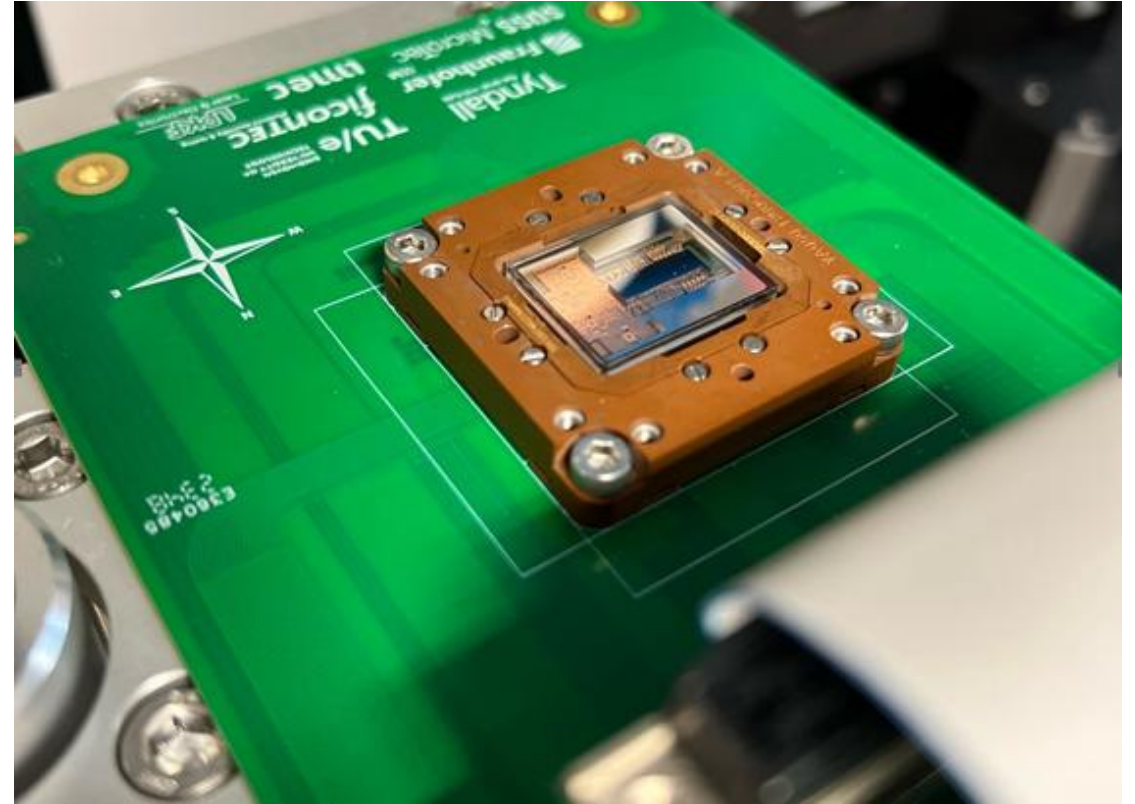
- scalable to large volumes

Reduction of test time per chip

- Target: >100 times reduction
- From 10's of **minutes/device** to **seconds/device**.

Open standards test framework

- of device design, measurement methods data handling
- 'first-time-right' designs





**When people share curiosity
and respect,
they build trust.**

**When trust meets ambition,
innovation follows naturally.**



Mutual Respect | Shared Ambition | Long Term Partnership



**Photonic Integration
Technology Center**